# ECR #: 33
# Title: Coherent access and GART
# Release Date: May 12, 1997
# Impact: Clarification
# Spec Version: A.G.P. 1.0

**Summary:** Need to clarify the processor cache coherency requirements for A.G.P. transactions.

**Background:** This ECR provides a clarifying replacement for the "Coherency" paragraph in section 2.4

## Change Current Specification as shown:

Replace the subject paragraph with the following text.

**Coherency with processor cache**: Due to the high potential access rate on the A.G.P., it is not advisable from a performance perspective to snoop all accesses. Selective snooping in an integrated core logic architecture presents serious queue management problems, while the MP bus in an MP core logic architecture could well deal with selective snoops very easily. As a result, processor cache snooping on A.G.P. accesses is chipset dependent, and may not be counted upon in general. The exact coherency requirements for this interface specification are as follows:

Processor cache coherency must be guaranteed by the core logic for all PCI transactions (transactions initiated with the **FRAME#** signal) regardless of which bus segment (A.G.P. or PCI) they originate on. This is consistent with normal PCI operation. Coherency means that at the moment a PCI/A.G.P. memory request is serviced, the subject data are fully consistent with any valid contents of the processor caching mechanism (excluding processor write combining buffers) for any of the target locations in the access.

For A.G.P. transactions (transactions initiated with the **PIPE#** signal or on the de-multiplexed address bus, **SBA***x*), there are no specific coherency requirements, and behavior is chipset dependent. It is entirely possible that some implementations will return stale read data, or allow write data to be overwritten, e.g., by a processor cache write back. Other implementations may provide full coherency support. For this reason, **any device driver managing an A.G.P. device is required to insure that A.G.P. transactions targeted at cacheable memory are safe**. In practice, this caution applies mostly to A.G.P. transactions **outside** the GART address range, since memory allocated **inside** the GART address range by the normal A.G.P. memory allocation procedure will be of a cache type (e.g., USWC) consistent with the hardware's ability to support coherency. In general, an A.G.P. device driver may determine the level of chipset coherency support via the chipset ID available in the windows registry.